Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.020”**

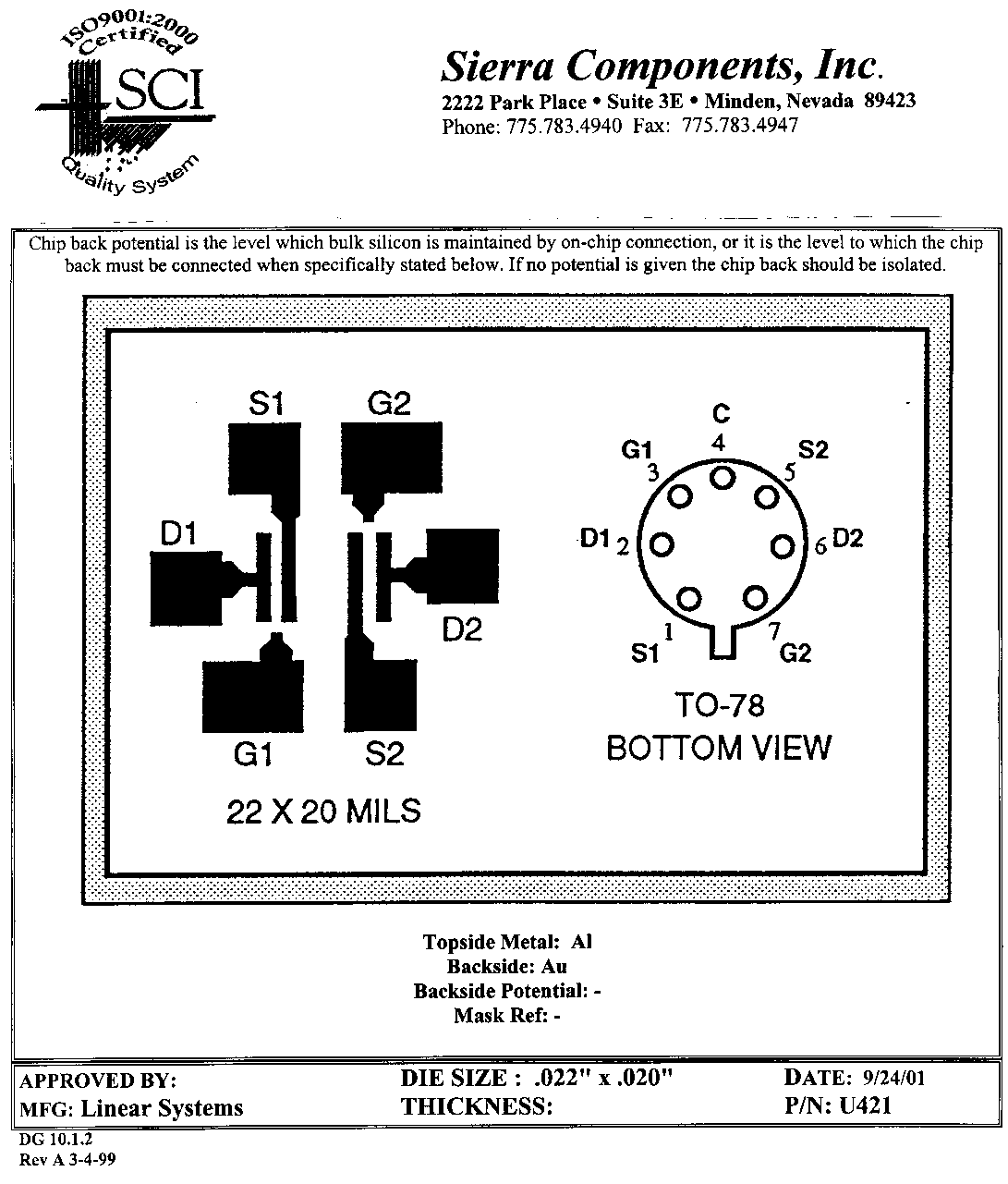
**.022”**

**G1 S2**

**S1 G2**

**D1**

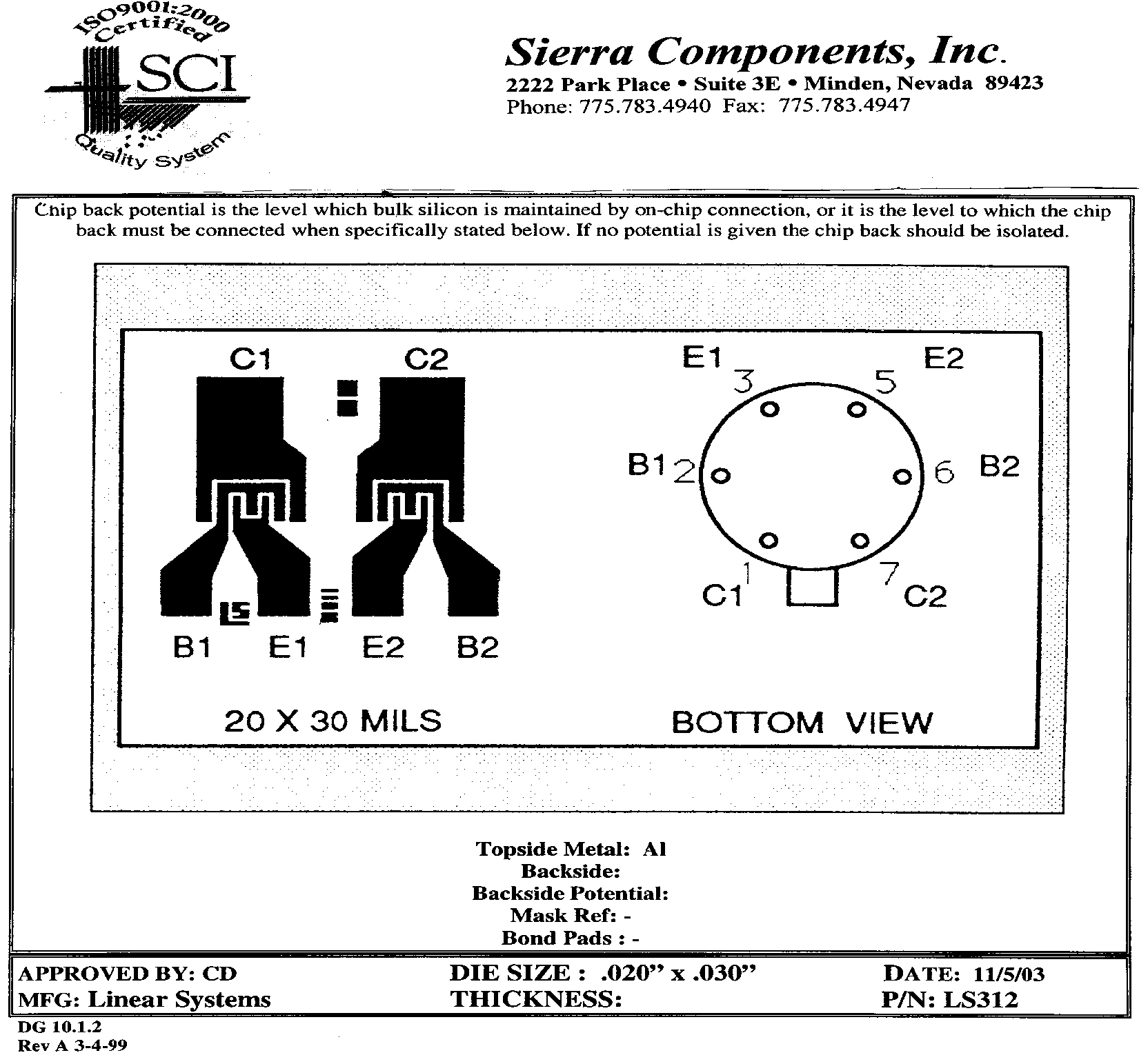
**D2**



**2011**

**JF**

**202DL**



**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: G = .003” X .0045” D/S = .003” X .003”**

**Backside Potential:**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .020” X .022” DATE: 3/3/17**

**MFG: LINEAR SYSTEMS THICKNESS .008” P/N: LS832**

**DG 10.1.2**

#### Rev B, 7/19/02